

FIG. 1 PRIOR ART

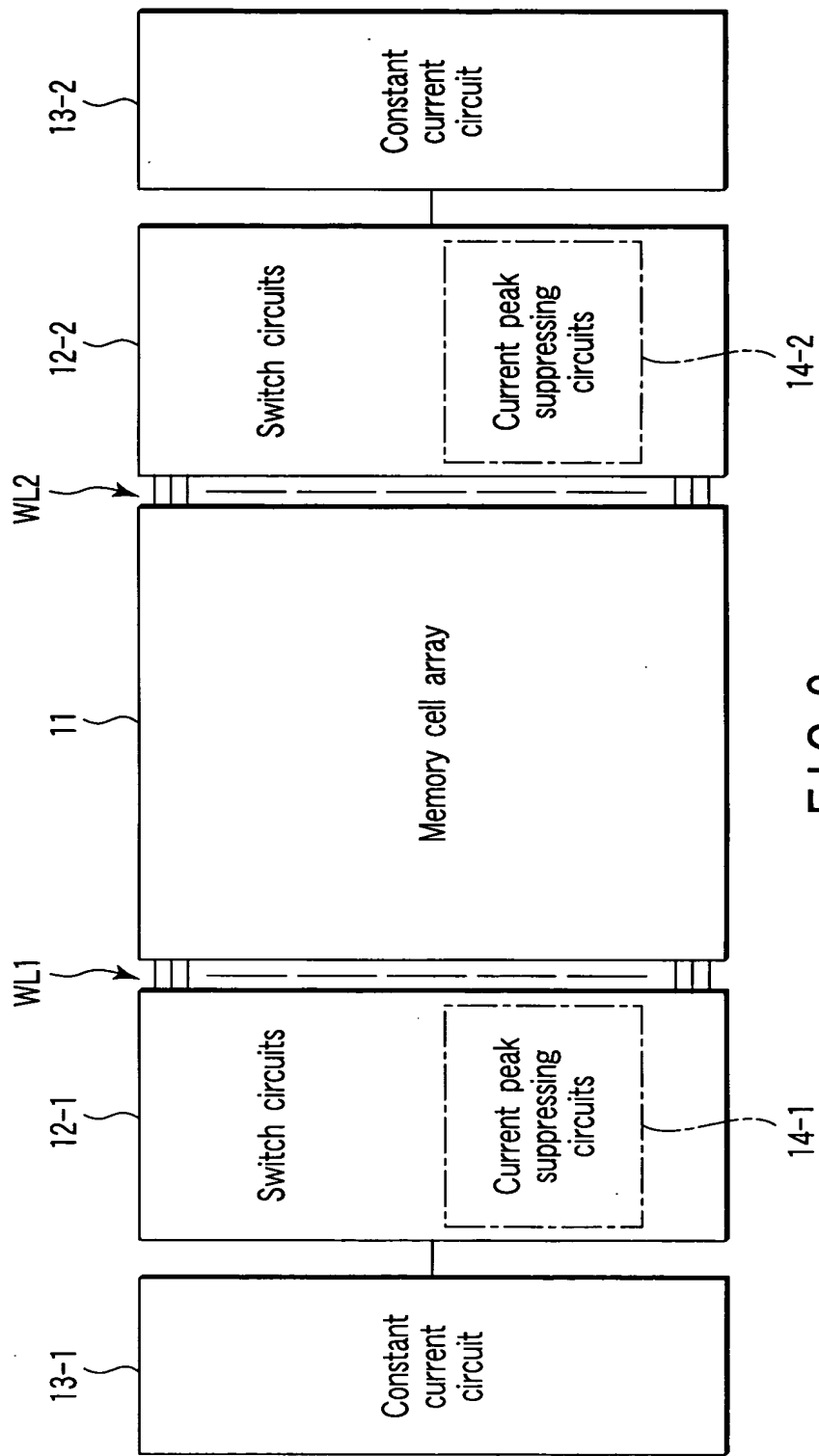


FIG. 2

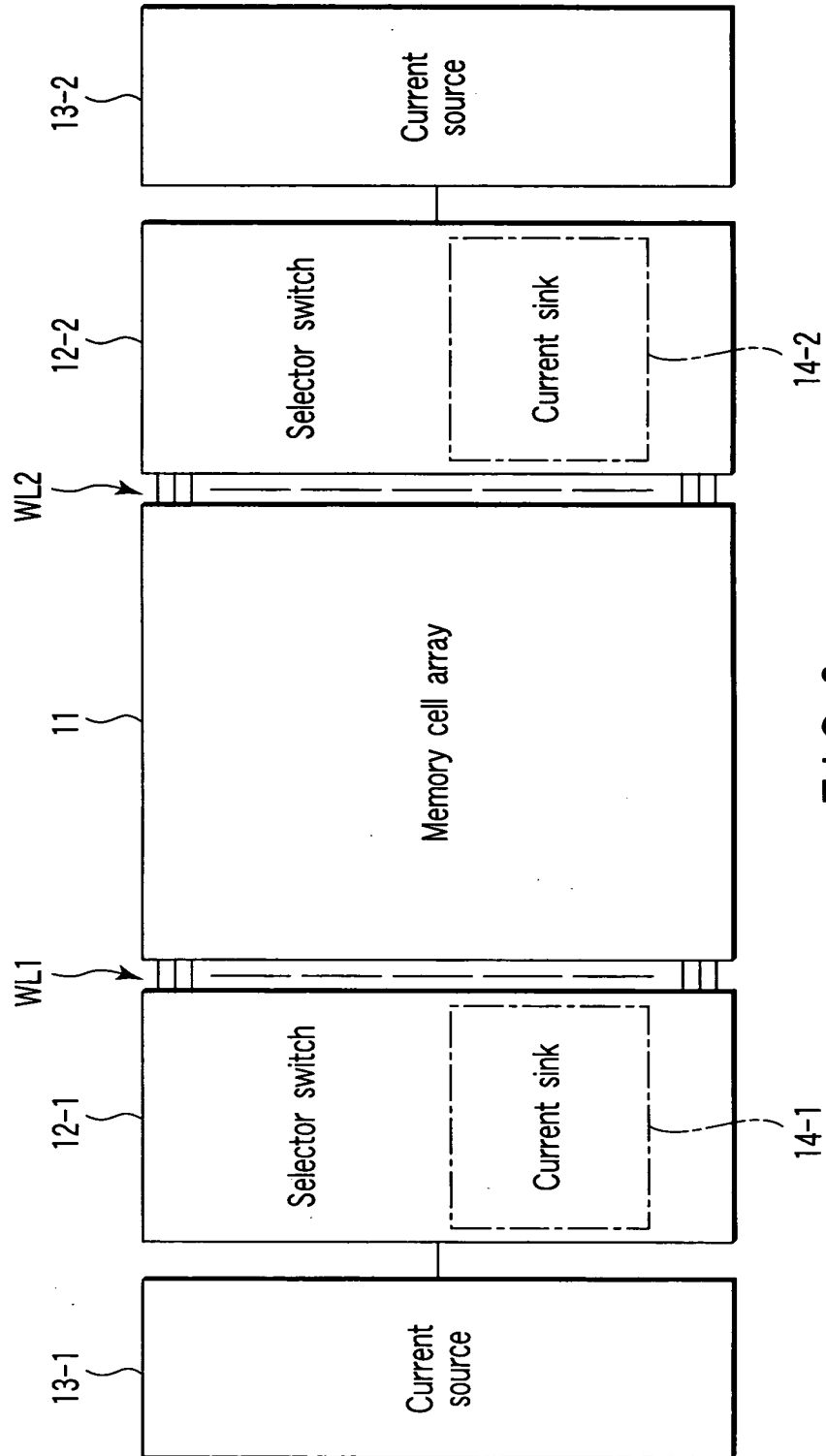


FIG. 3

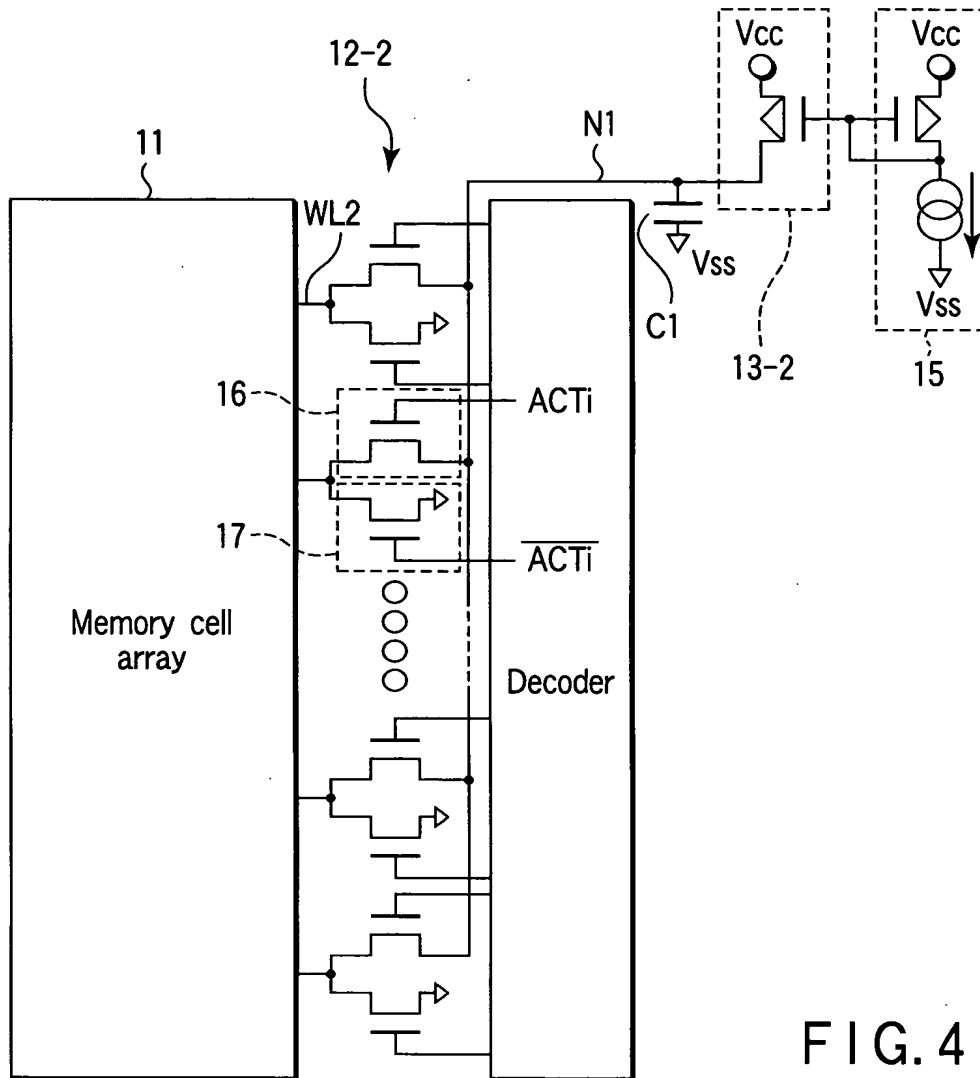


FIG. 4

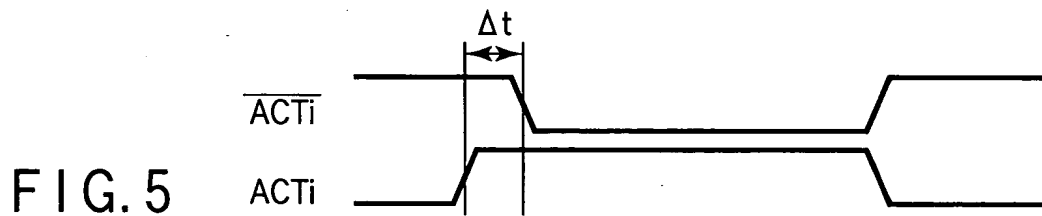


FIG. 5

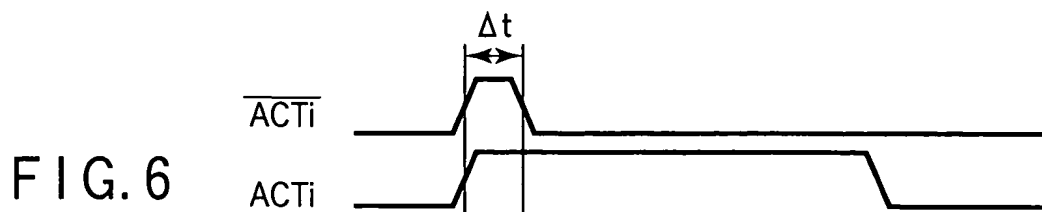


FIG. 6

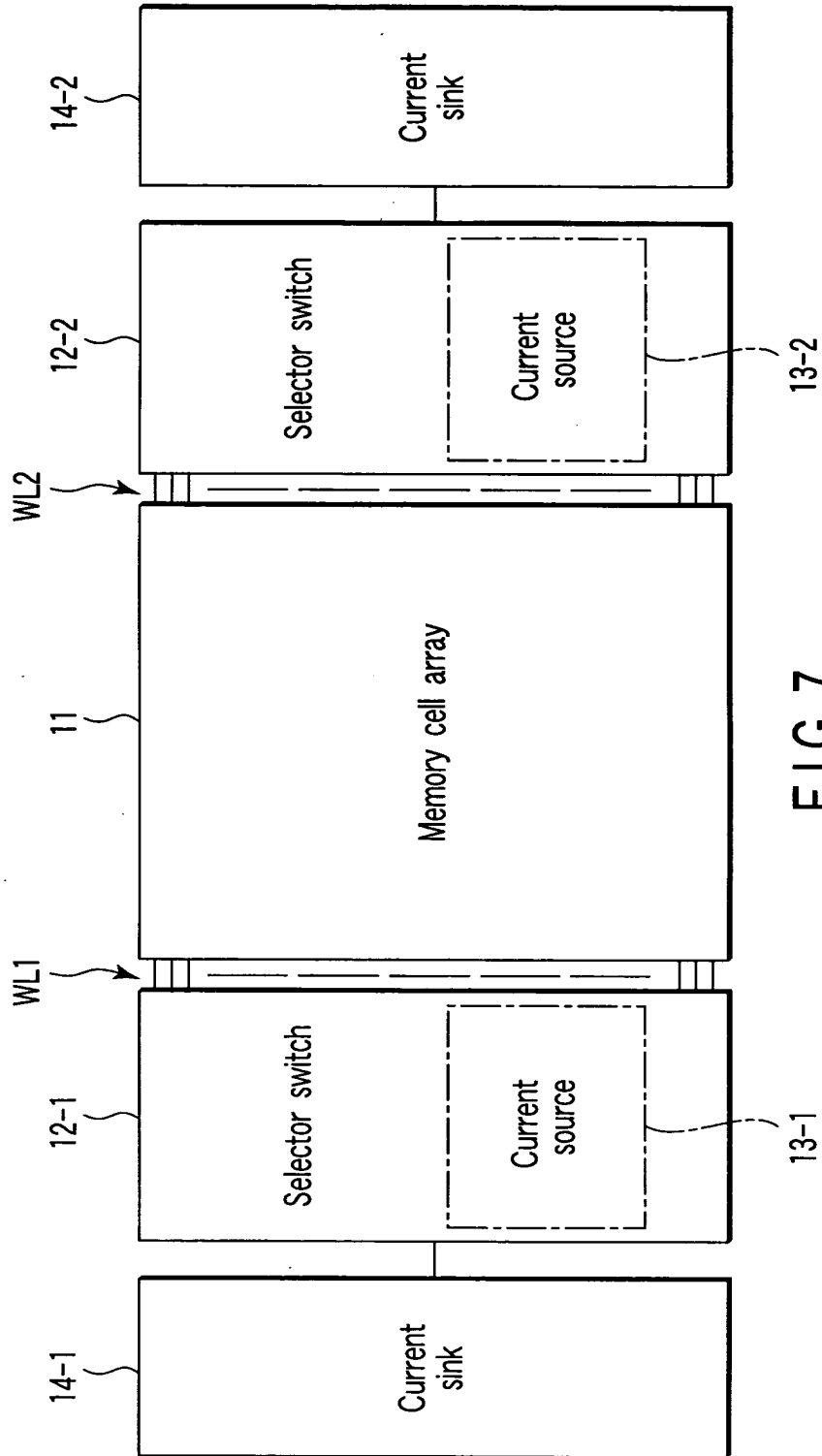


FIG. 7

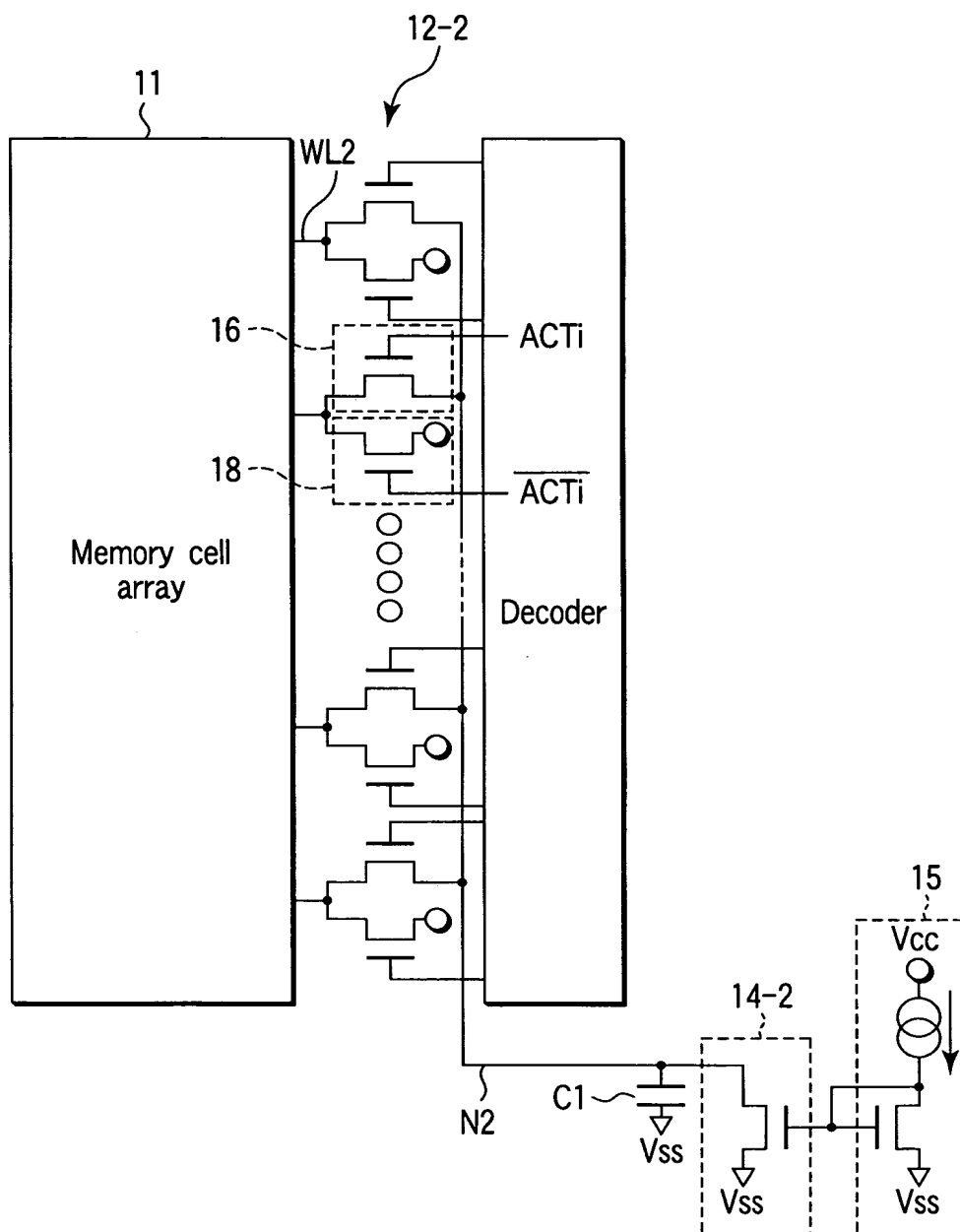


FIG. 8

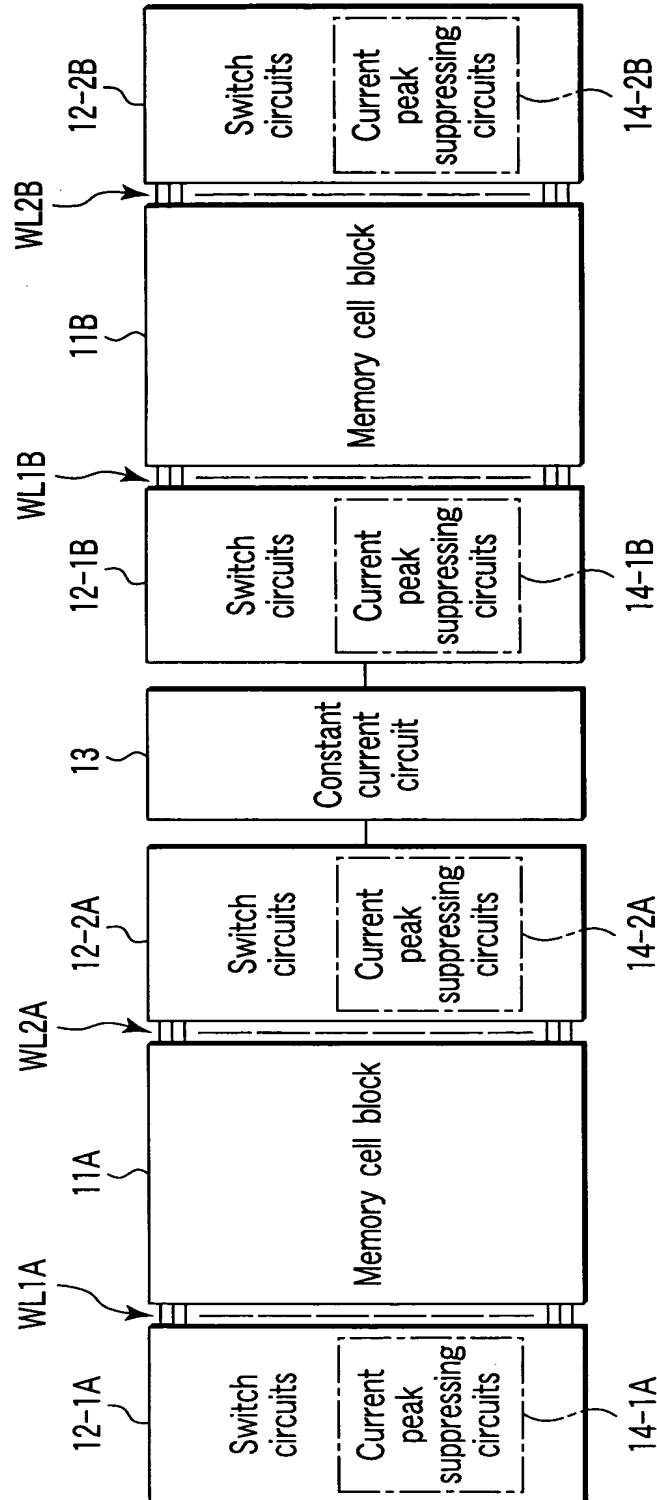


FIG. 9

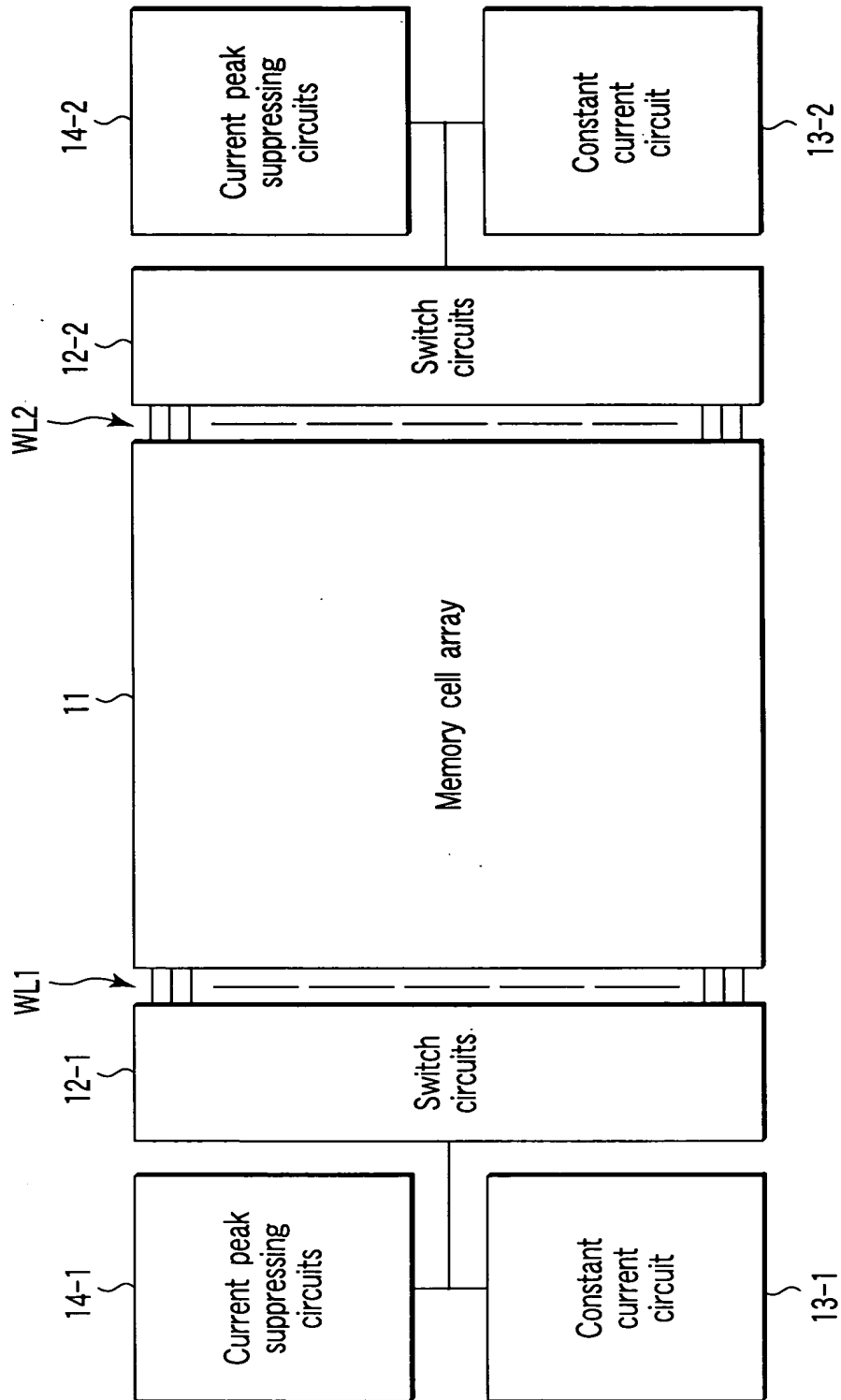


FIG. 10



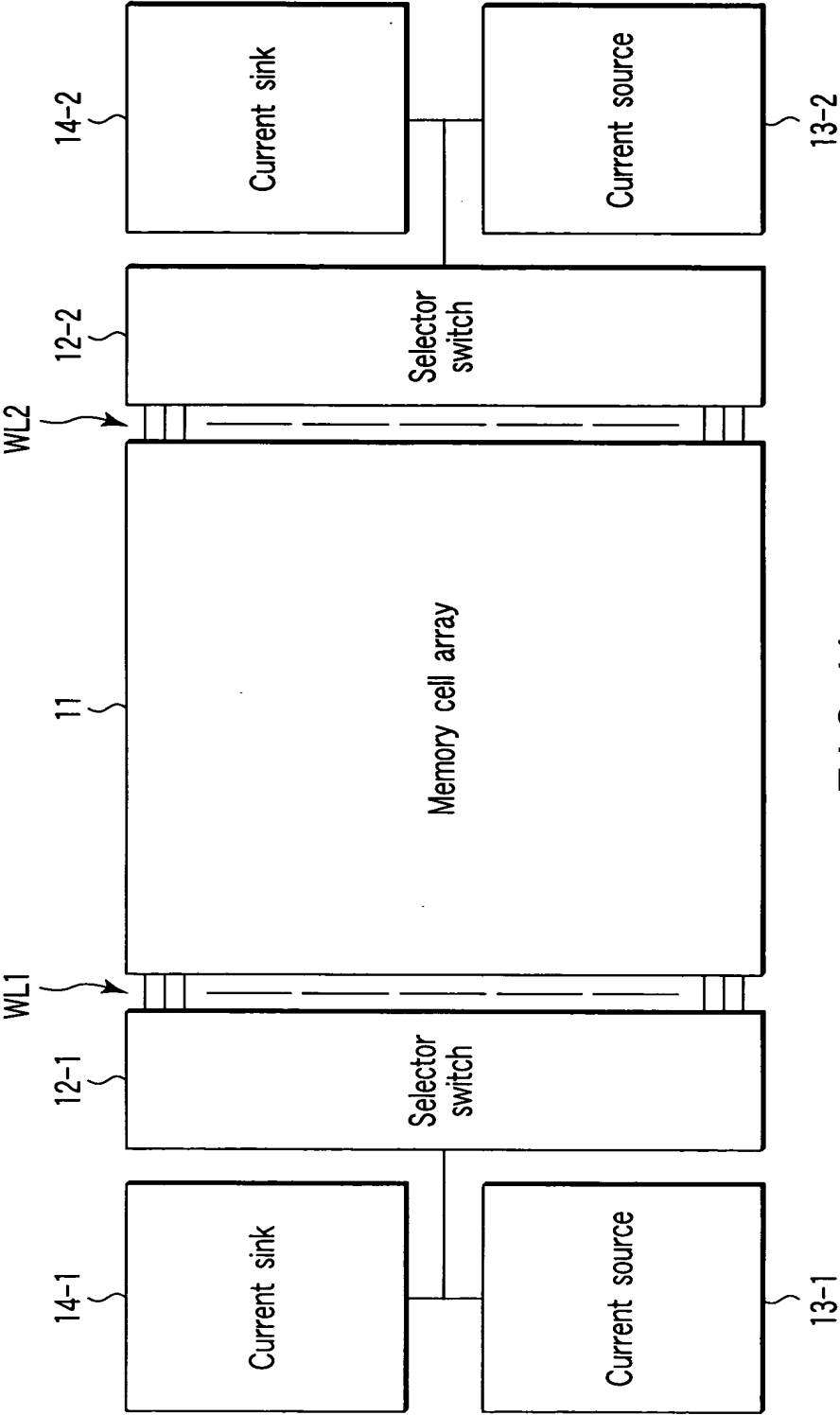


FIG. 11

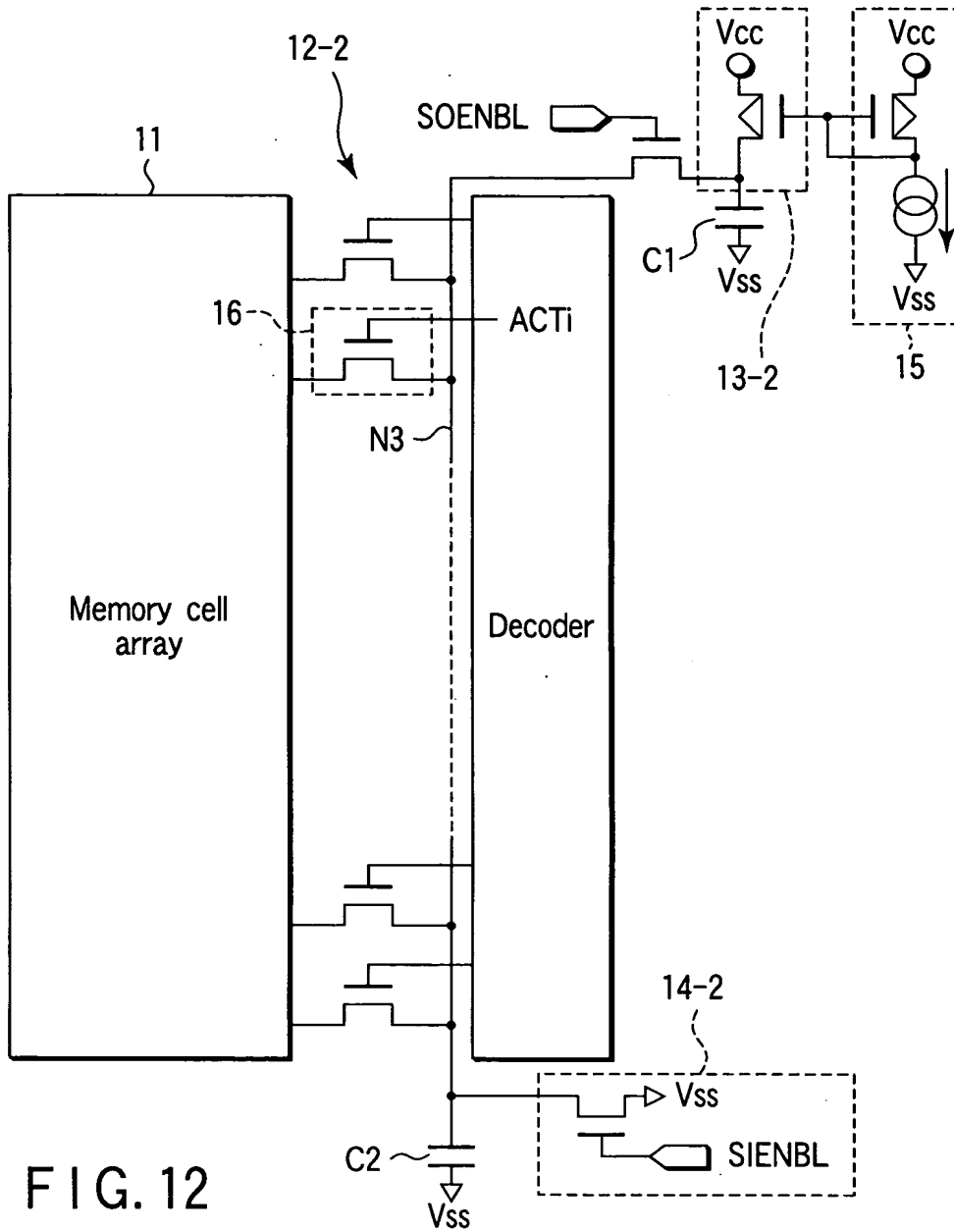
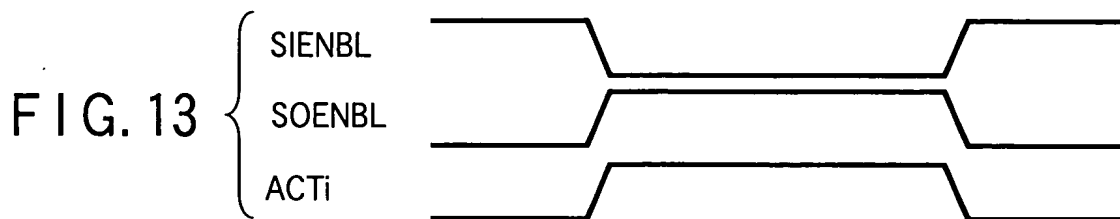
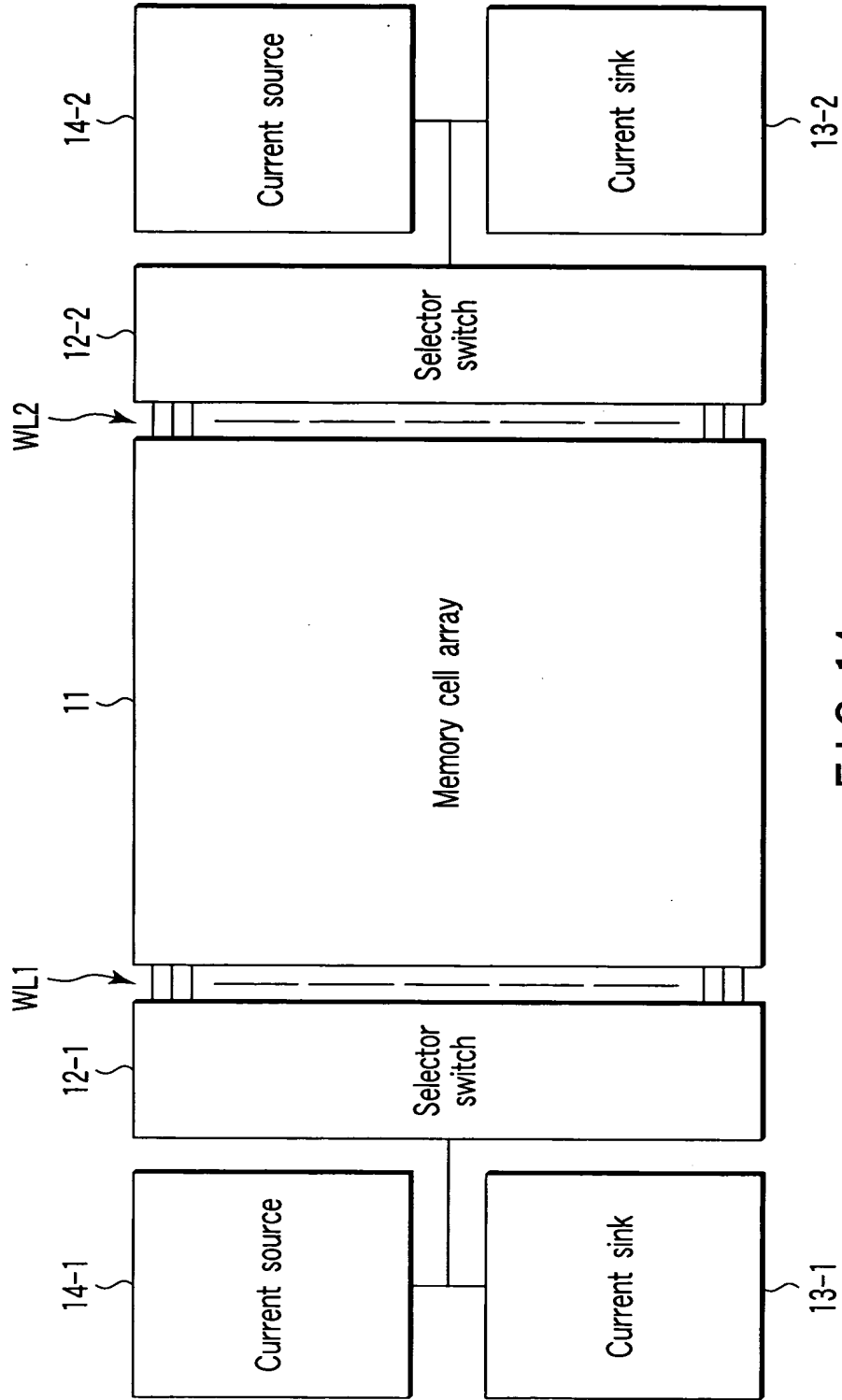


FIG. 12







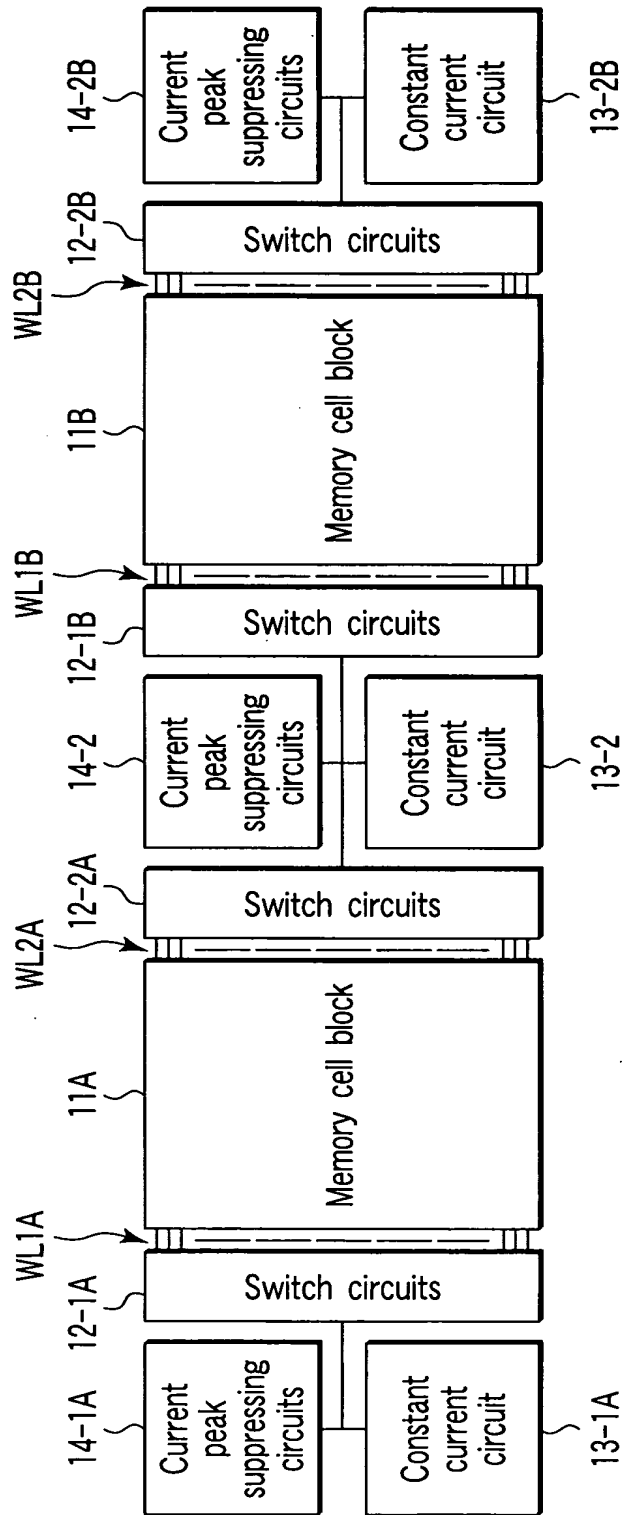


FIG.17

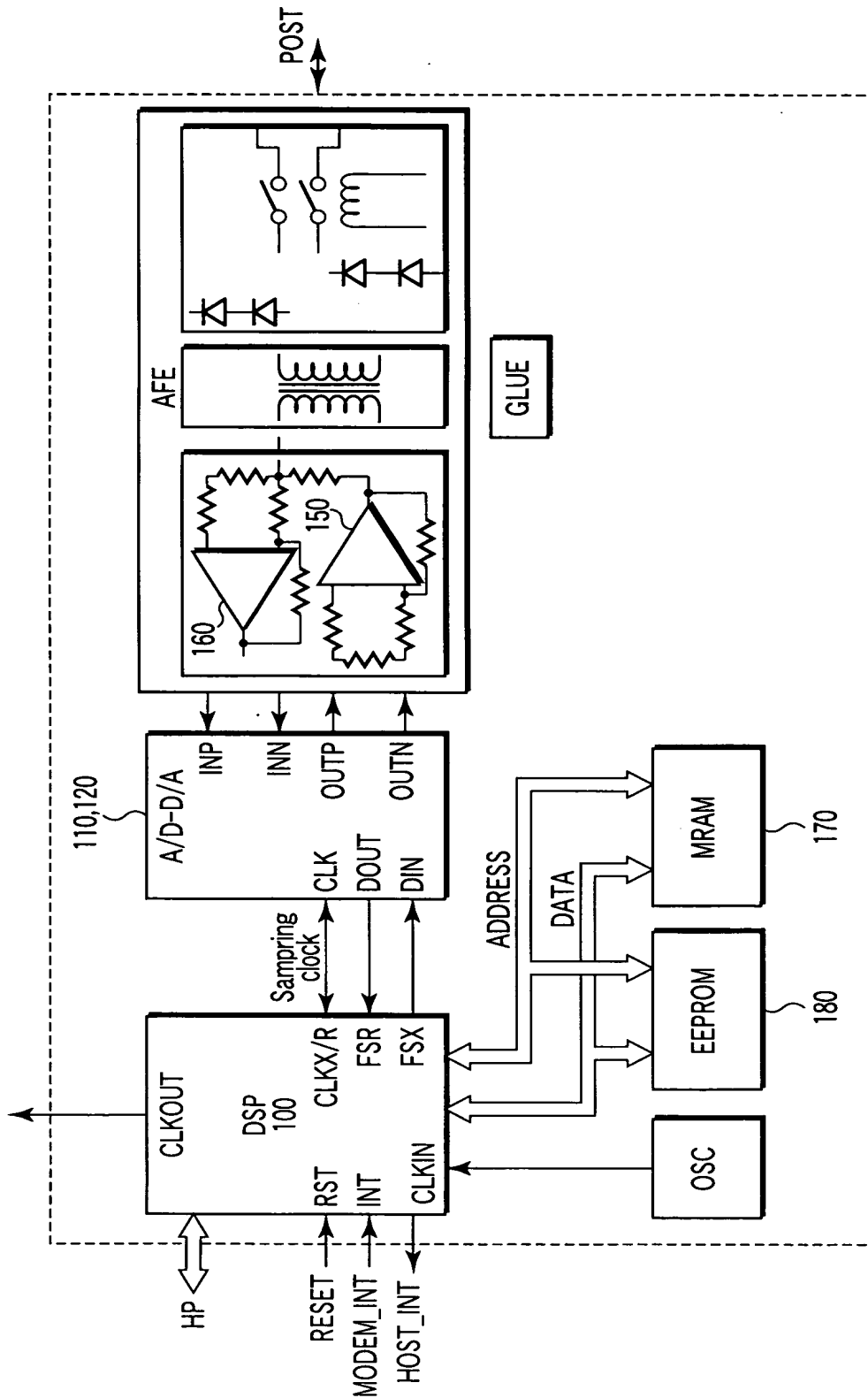


FIG. 18

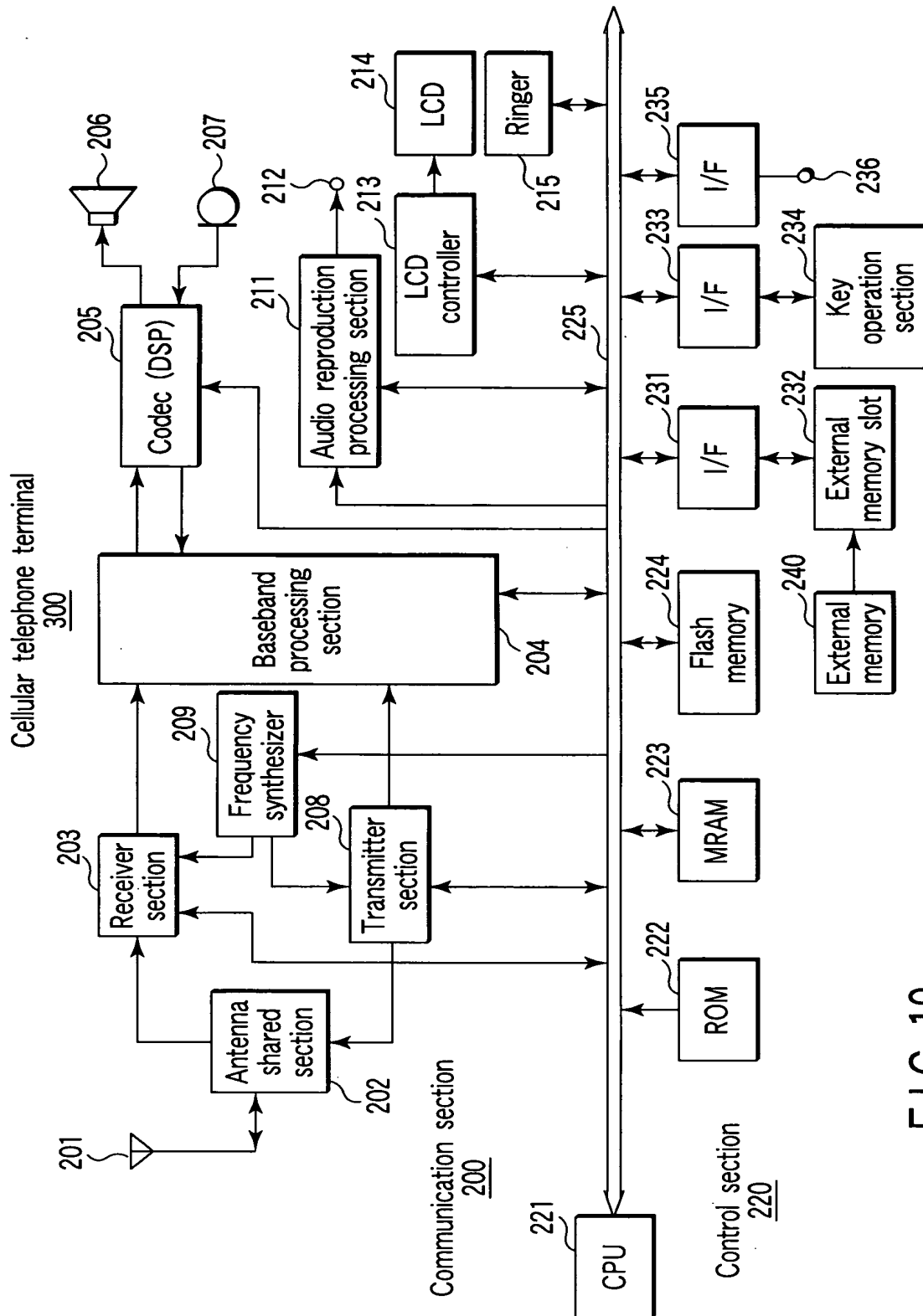


FIG. 19

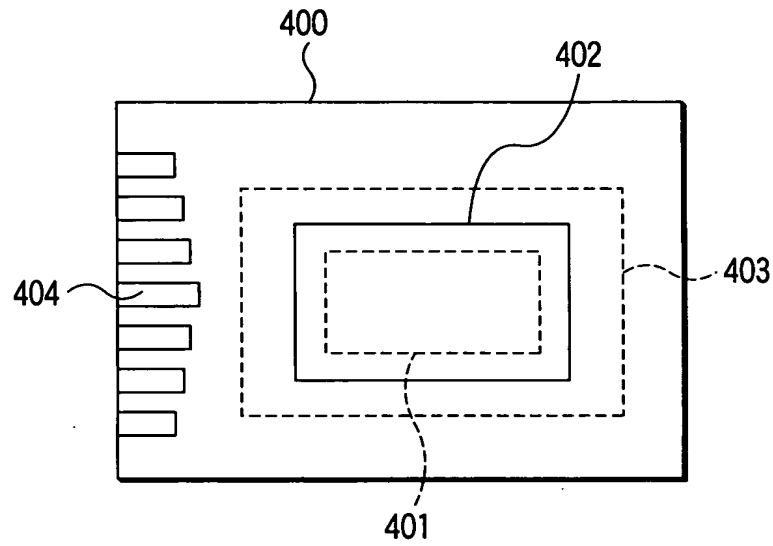


FIG. 20

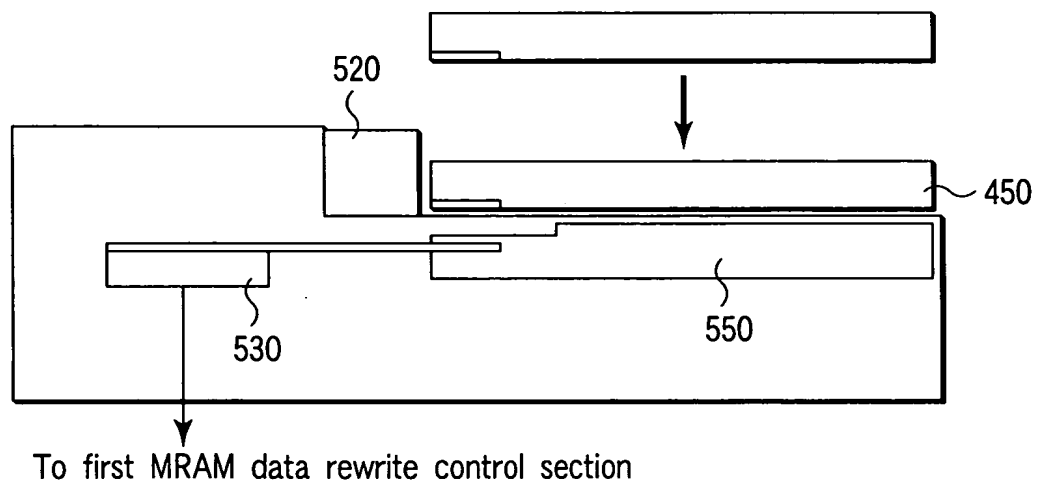


FIG. 23



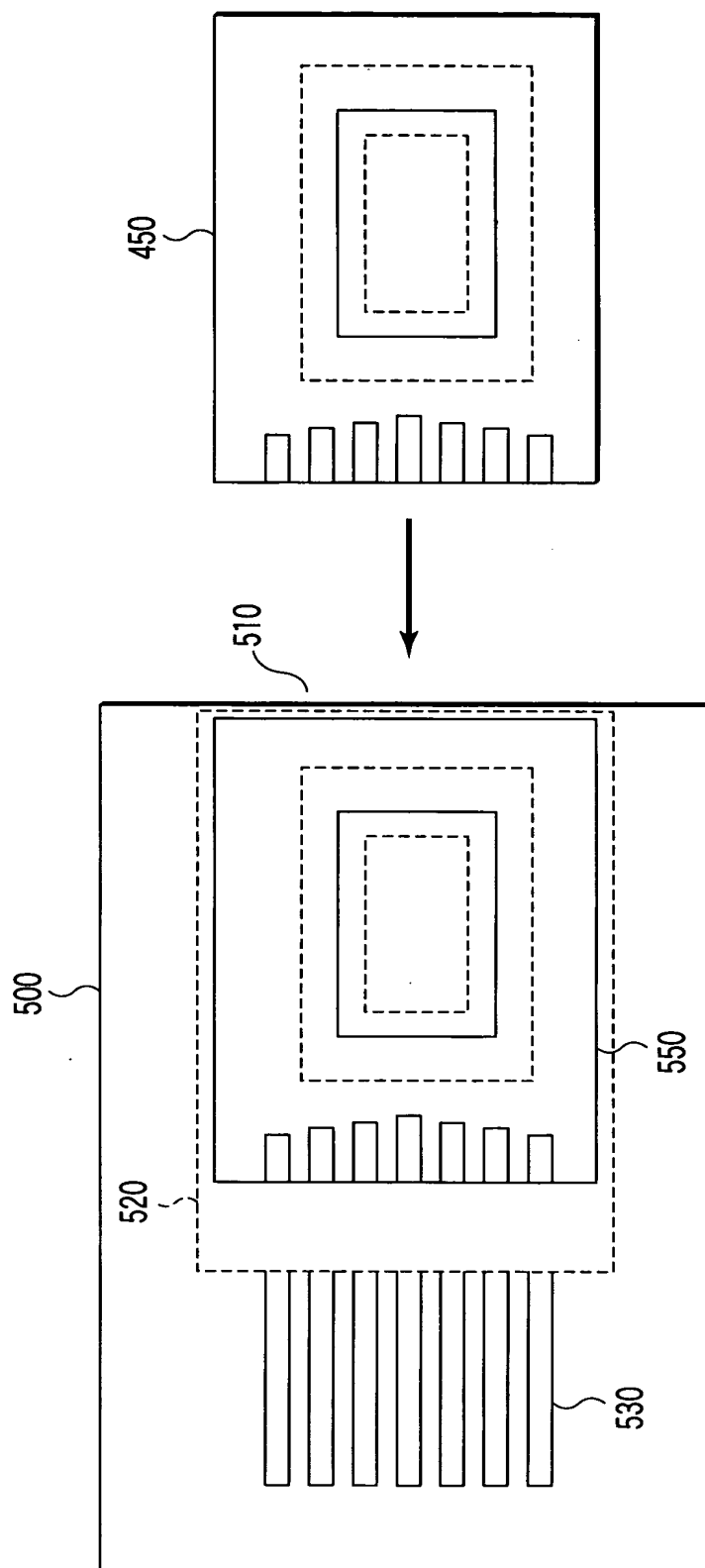


FIG. 21

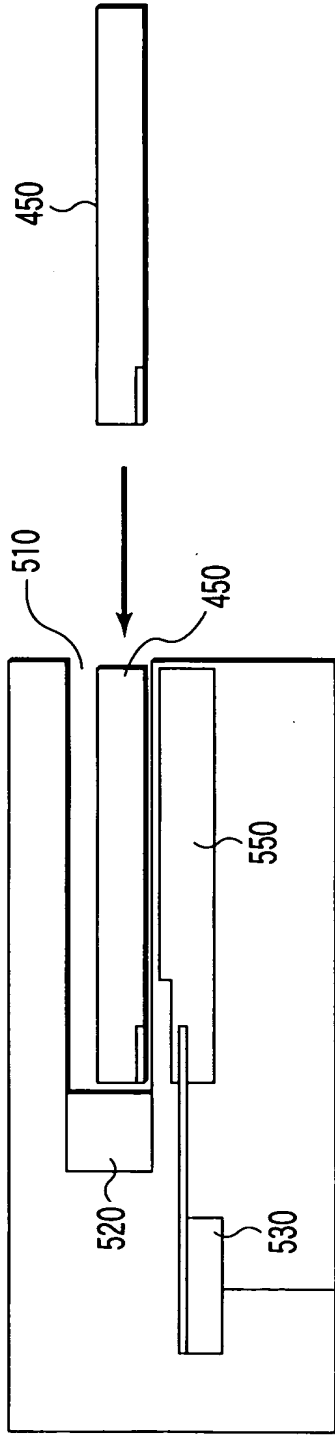


FIG. 22

To first MRAM data rewrite control section

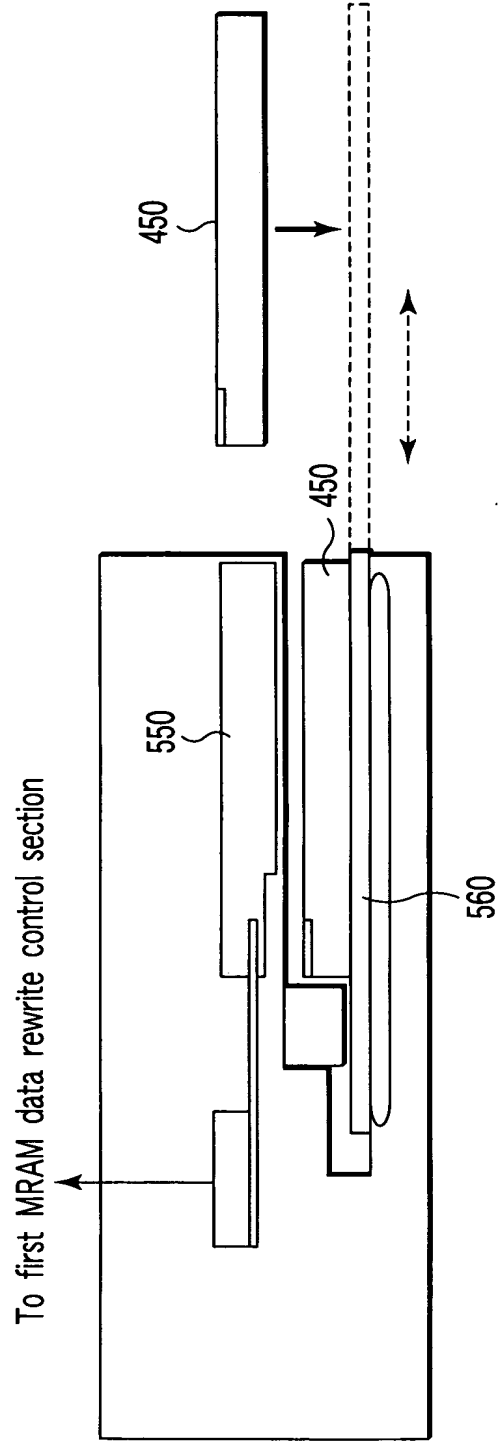


FIG. 24

To first MRAM data rewrite control section